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PATENT APPLICATION
DOCKET NO.: 200315314-1

AMENDMENTS TO THE DRAWINGS

The attached sheet of drawings (sheet no. 4/4) includes changes to FIG. 4. This drawing sheet, which includes FIG. 4 only, is in compliance with 37 C.F.R. §1.121(d) and replaces the original sheet no. 4/4. Block 406 of FIG. 4 has been amended so as to secure correspondence within the disclosure.

Attachments: Replacement Sheet

Annotated Sheet Showing Changes

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REMARKS

Claims 1-22 are presented for examination. Of the claims 1-22 currently pending, claims 1, 9 and 16 are in independent form.

Claims 1, 9 and 16 have been amended by way of the present response. No new matter is introduced hereby.

Support for the claim amendments of the present response may be found, *inter alia*, in FIGS. 1B and 3, for example, as well as the related description at Paragraphs [0012]-[0013] and [0021] through [0025] of the specification of the instant application.

Favorable reconsideration of the present application as currently constituted is respectfully requested.

Regarding Objections to the Drawings

In the present Office Action, the drawings are objected to because of certain informalities in Text Box 406 of Figure 4. Accordingly, Figure 4 has been appropriately amended. A replacement sheet (sheet no. 4/4) of drawings and an annotated sheet showing the changes are enclosed with this response. This objection is now believed to be moot.

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Regarding the Claim Rejections - 35 U.S.C. §112, Second Paragraph

Claims 1-22 stand rejected in the pending Office Action under 35 U.S.C. §112, Second Paragraph, as lacking antecedent basis for "said signal".

The Examiner also stated that "[I]t is not clear how the detection of a signal's edge can be responsive to the detection of the assertion of that same signal."

Applicant respectfully submits that these rejections have been overcome or otherwise rendered moot by way of the present response wherein base claims 1, 9 and 16 have been amended appropriately.

Regarding the Claim Rejections - 35 U.S.C. §102(b)

(I) Marchelli

Claims 1-22 are rejected in the pending Office Action under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 4,300,100 to Marchelli (hereinafter the *Marchelli* reference). In connection with these rejections, the Examiner has commented as follows with respect to base claim 1:

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Marchelli's Fig. 4 shows a system for detecting an edge of a data signal (Clx) carried on an observability bus, the system comprising:

a first performance counter (FF') connected to receive said data signal, said first performance counter being operable to assert a trigger signal (d) in response to detecting an assertion of said data signal (clearly shown in Fig. 4a); and

a second performance counter (G and FF'') connected to receive said data signal and said trigger signal, wherein said second performance counter detects said edge responsive to detecting said assertion of said data signal (when signals Cl) (and b are asserted so is the output f) and a logic level in said trigger signal that is a complement to a logic level associated with said assertion of said signal (insofar as understood based on the 112 rejection above) as called for in claim 1.

Substantially identical reasons are also provided in the pending Office Action with respect the rejection of base claims 9 and 16.

Applicant respectfully submits that the pending \$102(b) rejections as set forth above have been overcome or otherwise rendered moot by way of the present amendment and offers the following discussion as support. As defined by the base claim 1, an embodiment of the present disclosure is directed to a system for detecting an edge of a data signal carried on an observability bus. As currently constituted, the claimed system

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involves, *inter alia*, a first performance counter connected to receive the data signal, the first performance counter being operable to assert a trigger signal in a given clock cycle in response to detecting an assertion of the data signal in the previous clock cycle. The system further involves a second performance counter connected to receive the data signal and the trigger signal, wherein the second performance counter is operable to detect the edge in the data signal based on the assertion of the data signal and a logic level in the trigger signal that is a complement to a logic level associated with the assertion of the data signal.

By way of the present amendment, base claims 9 and 16 contain similar features. Claim 9 is directed to an embodiment of a method for detecting an edge of a data signal carried on an observability bus. Likewise, claim 16 is directed to another embodiment of a system for detecting an edge of a data signal carried on an observability bus.

The *Marchelli* reference is directed to providing a circuit arrangement for correlating the operation of two or more multistage counters (each counter possibly including a primary

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and secondary chain of binary stages) which are driven substantially at the same frequency but having indeterminate phase relationships. See column 1, lines 45-50. Figure 4 of this reference illustrates a generic correlation circuit and Figure 4a illustrates exemplary signals that are employed in this circuit. These Figures are reproduced herein for convenience.

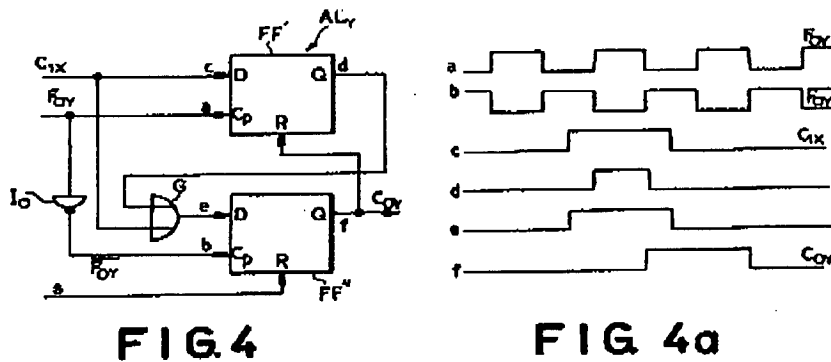


FIG. 4

FIG 4a

It appears that signals *c* and *d* of *Marchelli* are being equated with the data signal and trigger signal as claimed by Applicant. However, it is clear from the Figure 4a of *Marchelli* that signal *d* is not asserted in a given clock cycle in response to detecting an assertion of signal *c* in the previous clock cycle, as is

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currently recited in claim 1. Further, *Marchelli* does not disclose or suggest that the logic levels of signals *c* and *d* are compared to each other in order to detect an edge in the data signal, as is also recited in claim 1.

Based on the foregoing, Applicant respectfully submits that base claim 1 is not anticipated or suggested by the *Marchelli* reference, and is therefore in condition for allowance. Base claims 9 and 16 contain the same distinguishing features and are also in condition for allowance. Claims 2-8 depend from the base claim 1 and introduce additional limitations therein. Likewise, claims 10-15 depend from base claim 9 and claims 17-22 depend from base claim 16, each introducing additional limitations therein. Accordingly, these dependent claims are also believed to be in condition for allowance over *Marchelli*.

(II) Negi

Claims 1-22 are also rejected in the pending Office Action under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,600,695 to Negi (hereinafter the *Negi* reference). In

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connection with these rejections, the Examiner has commented as follows with respect to base claim 1:

Negi's Fig. 5 shows a system for detecting an edge of a data signal (4) carried on an observability bus, the system comprising:

a first performance counter (1-1) connected to receive said data signal, said first performance counter being operable to assert a trigger signal (CO) in response to detecting an assertion of said data signal (clearly shown in Fig. 6); and

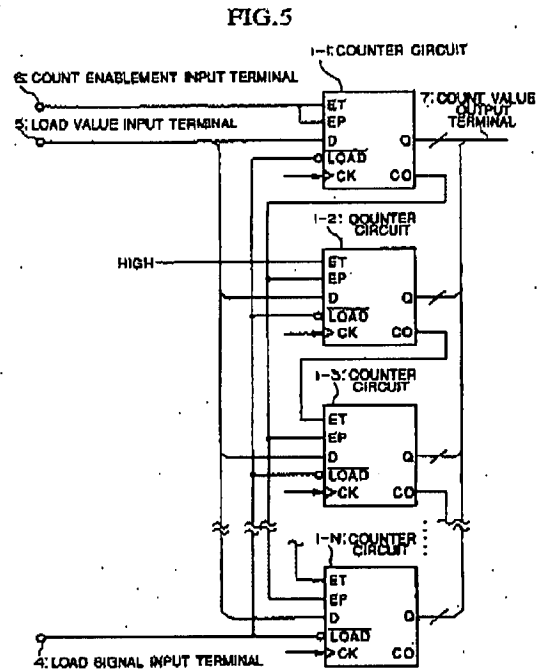
a second performance counter (1-2) connected to receive said data signal and said trigger signal, wherein said second performance counter detects said edge responsive to detecting said assertion of said data signal (when signals 4 and CO of 1-1 are asserted so is the output CO of 1-2) and a logic level in said trigger signal that is a complement to a logic level associated with said assertion of said signal (insofar as understood based on the 112 rejection above) as called for in claim 1.

Substantially identical reasons are also provided with respect the rejection of base claims 9 and 16 on the basis of Negi.

Applicant again respectfully submits that the pending §102(b) rejections as set forth above have been overcome or otherwise rendered moot by way of the present amendment. The Negi reference is directed to a counter circuit that is able to perform counting operations no matter what kind of value has been

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loaded into the circuit. Figure 5 of Negi discloses an embodiment of a counter circuit that Negi considers prior art and Figure 5 discloses a timing diagram relating to various signal employed in the circuit of Figure 5. Signal CO of Counter Circuit 1-1 of Figure 5, which appears to be equated with the claimed trigger signal, corresponds to Counter Circuit Carry Output CO 1-1 of Figure 6. Load Signal Input 4 appears to be equated with the claimed data

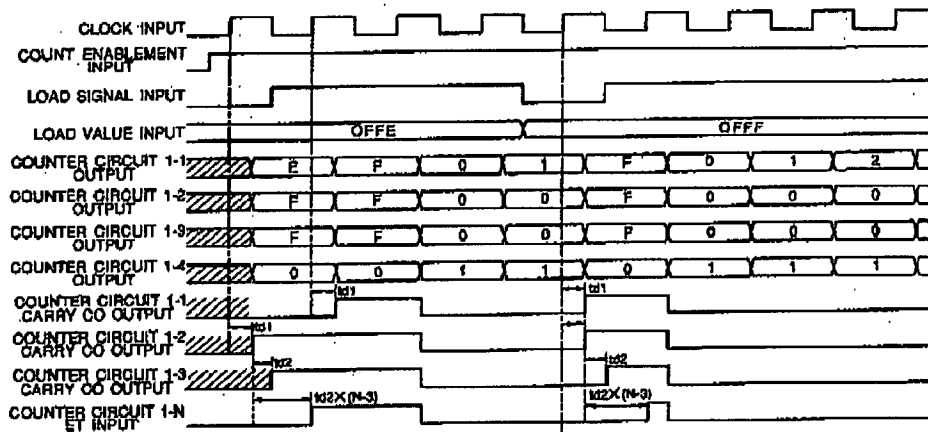


signal whose edge is being detected. As shown in Figure 6 below, signal CO of circuit 1-1 is not asserted in a given clock cycle in response to detecting the assertion of Load Signal Input 4 in the previous clock cycle, as is currently recited in claim 1. Neither does Negi disclose or suggest that the logic level values of these signals are compared to each other in order to detect an

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edge in the data signal (i.e., the Load Signal Input signal), as is also recited in claim 1.

FIG.6



Based on the foregoing, Applicant respectfully submits that base claim 1 is not anticipated or suggested by Negi, and is therefore in condition for allowance over this reference. Base claims 9 and 16 contain the same distinguishing features and are also in condition for allowance. Claims 2-8 depend from the base claim 1 and introduce additional features therein. Likewise, claims 10-15 depend from claim 9 and claims 17-22 depend from base claim 16, each introducing additional features therein.

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Accordingly, these dependent claims are also believed to be in condition for allowance over *Negi*.

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SUMMARY AND CONCLUSION

In view of the fact that none of the art of the record, whether considered alone or in combination discloses, anticipates or suggests the pending claims, and in further view of the above remarks and amendments, reconsideration of the Action and allowance of the present patent application are respectfully requested and are believed to be appropriate.

Respectfully submitted,

Dated: _____

8/31/2007



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Response Dated 08/31/2007
In reply to Office Action of May 31, 2007
ANNOTATED SHEET SHOWING CHANGES

4/4

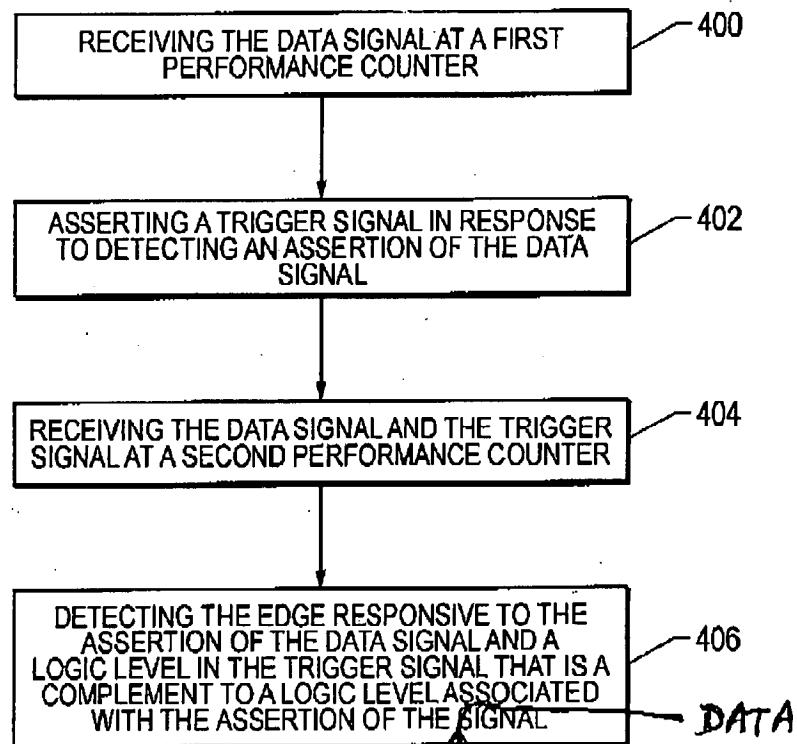


FIG. 4

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